REMARKS

Claims 2-7, 9-13, 15, 17 and 25 are pending. By this Amendment, claims 1, 8, 14, 16 and 18-24 are cancelled without prejudice to or disclaimer of their subject matter, and claims 2, 4, 6, 9-11, 13, 15 and 17 are amended. Claim 25 is added.

Claim 6 is amended to clarify that the first and second rows of pixels are arrayed along spaced and separate lines to preclude construing the device as having first and second rows of pixels arrayed along collinear lines. Claim 6 is also amended to incorporate the subject matter of dependent claim 8, and claim 8 is thereafter cancelled. Claims 9-11, otherwise depended on claim 8, have been amended to depend on claim 6. Claims 4, 13 and 17 have been amended to clarify that the pixel includes either a photodiode, a pinned photodiode or both (i.e., an inclusive or instead of an exclusive or). Claim 15 is amended to clarify that the summation is performed on the same chip as the readout registers. Claim 25 is added to specify that end elements of the readout registers are coupled to function as a single output node, and claims 2-5 amended to depend directly or indirectly on new claim 25.

The Office Action rejects claims 1-17 under 35 U.S.C. 102(b) as anticipated by Yasuda et al. '099.

As to originally filed claim 2 (and all claims dependant thereon) and originally filed claim 6 (and all claims dependant thereon), this rejection is respectfully traversed. Yasuda et al. '099 does not disclose, teach or suggest a device that includes "a first clocking structure disposed over and transverse to the plurality of first channel structures, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode" as specified in originally filed claims 2 and 6 and therefore contained in all claims dependant thereon. This feature (as generally disclosed in the present application, e.g. FIG. 2) provides the present invention with distinct advantages over the prior art as described in the application.

As to originally filed claim 15, this rejection is respectfully traversed. Yasuda et al. '099 does not disclose, teach or suggest a device that includes "a summation circuit to combine serial outputs from the first and second readout registers" as specified in claim 15. This feature (as generally disclosed in the present application, e.g. page 8) provides the present invention with distinct advantages over the prior art as described in the application.

If this rejection is applicable to the present claims, this rejection is respectfully traversed. Yasuda et al. '099 does not disclose, teach or suggest a device that includes "first and second rows of pixels defined along respective first and second lines, the first line being spaced from and parallel to the second line" as specified in claim 6 and therefore contained in all claims dependent thereon. To the contrary, Yasuda et al. discloses that sensor 12 includes plural sensor units arranged to form a straight line. See column 4, lines 32-34 and column 9, lines 9-13.

The Office Action rejects claims 1, 6 and 14 under 35 U.S.C. 102(e) as anticipated by Hirama et al. '299.

Claims 1 and 14 are not pending. If applicable to present claim 6, this rejection is respectfully traversed. Hirama et al. '299 does not disclose, teach or suggest a device that includes both (1) "a first clocking structure disposed between the first row of pixels and the first readout register, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode" and (2) "a second clocking structure disposed between the second row of pixels and the second readout register, wherein the second clocking structure includes a transfer gate electrode and a delay well electrode" as specified in claim 6 and therefore contained in all claims dependent thereon.

Accordingly, withdrawal of all rejections is earnestly solicited.

The Commissioner is hereby authorized to charge or credit any deficiency in fees due caused by this amendment to Deposit Account No. 04-1425.

In view of the present amendments and remarks, it is respectfully submitted that this application is in condition for allowance. Prompt reconsideration and allowance are earnestly solicited. If the examiner believes that any further action is needed to place the application in condition for allowance, he is invited to contact the under subscribed representative at the telephone number noted.

Respectfully submitted,
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